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Case Study

System Architecture and Implementation of a Display Enhancement Standard Algorithm

Design Scope

- Hardware Architecture to retrofit an HDR Algorithm into an existing DTV SoC, Frame Rate Controller based platform
- Software Hardware Partitioning
- High speed LVDS and VBY1 Interface
- Optimum conversion of MATLAB -> C Language -> FPGA RTL
- RTL design and verification
- Integrated NIOSII
- Final Product Testing
- Subsequent ASIC IP development

Client

- **Tier 1 Company** which designs and manufactures audio and imaging products for the cinema, television, broadcast and entertainment industries

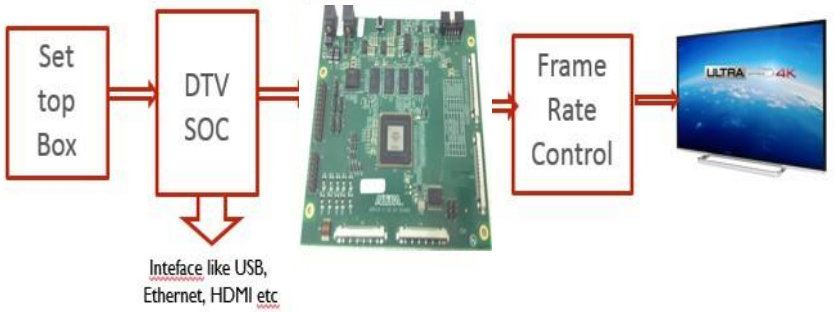
Tools/Technologies

- NCSIM, RTL Compiler, DC, Altera Quartus2

Solution/Highlights

Execution Highlights

- Multi-location team
- Interface with High – Speed LVDS and VBY1 interface
- Challenge in effective process of video/image at maximum speed of UHD @ 30Hz
- Capable of providing 40 times more brightness than a conventional TV.
- Delivers up to 1000 times more contrast to reveal depth and detail.
- Smooth gradients reveal nuances in rich detail.



THANK YOU

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