SUCCESS STORY

Development of an Automotive SoC

SoC ARCHITECTURE

INTRODUCTION

A niche engineering company developing an Automotive chip approached Ignitarium for architecture design and verification services of their radar SoC.

The new SoC is aimed to be used in Level 1 to Level 3 Autonomous Driver Assist Systems. The SoC which is a combination of a digital and analog die is intended to be ASIL-B certified with the processor subsystem meeting ASIL-D safety standards.

Service in Focus

SEMICONDUCTOR DESIGN SERVICES

Industry

Automotive - ADAS

Challenge

Automotive SoC Architecture and FuSa Compliance

Scope

- Architecture, SoC integration & Verification
- IP designs

THE CHALLENGE

Ignitarium was chosen as the architect and implementation partner for the processor subsystem. The functional and safety requirements along with hardware specifications had to be converted into an architecture and microarchitecture and further the design, verification, platform software development and validation had to be performed.

IGNITARIUM'S APPROACH

Ignitarium through its deep expertise in Automotive processor-based designs, defined the architecture of the dual Cortex R5 based ASIL-D safety island. Ignitarium made significant contribution in the architecture, design and verification of chip level functional safety features.

ARM Coresight based debug architecture ensured a rich debug environment including CPU and bus interconnect trace capabilities. Life cycle management was designed as per customer requirements and security requirements of the ASIC were also addressed.

Ignitarium was actively involved in DFMEA and FMEDA cycles to ensure ASIL-B compliance at chip level. Further, Ignitarium was involved in the verification of the processor subsystem, Analog Digital interface design and design of Digital FFT IPs. Our software teams are tasked with platform software development which has to be compliant to AUTOSAR standards and further in silicon validation.

4+

year business relationship

ASIL-B SoC with ASIL-D safety island for ARM Cortex R5F based CPU sub-system

6 CPUs supported

ARM Cortex M0+, R5F, Tensilica P5

BUSINESS IMPACT

- Architectural intervention and safety design implementation
- ISO9001 certified design processes to aid ease of certification
- System perspective of looking at both hardware and software aspects of the design

Looking for SoC Design and Verification services?

Drop us a line to get in touch with our experts.

Contact Ignitarium at info@ignitarium.com